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Group IV semiconductor nanowire arrays: epitaxy in different contexts

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Abstract
Epitaxy can be used to direct nanowire deposition and to influence the crystallographic orientation of nanowires during their nucleation and growth via the vapor–liquid–solid mechanism. We have investigated rapid thermal chemical vapor deposition of epitaxial Ge nanowires and have used it to separately study nanowire nucleation and growth. This work has provided important insights into deep-subeutectic Ge nanowire growth using Au catalyst particles. Germanium nanowires have also been studied as the cores in epitaxial Ge core/Si shell nanowires. We have studied the conditions under which strain-driven surface roughening and dislocations formation occur in these coaxial nanowire heterostructures. Our results indicate that suppression of Si shell surface roughening can lead to fully strained, coherent core/shell nanowires. Recently, we have used vertical arrays of Ge $\langle 1\,1\,1 \rangle$ nanowires grown at low temperatures on Si substrates to seed liquid-phase epitaxy of large-area amorphous Ge islands above the substrate surface. This work demonstrates a potential approach for dense vertical integration of Ge-based devices on Si substrates, for on-chip optoelectronics or 3D integrated circuit applications.

1. Introduction

Three-dimensional (3D) integration and the combination of different material systems are central themes of electronics research. Recently, silicon and germanium nanowires (NWs) have attracted great interest as molecular-scale device components that can be compatible with Si CMOS processing and that permit three-dimensional circuit architectures, have high performance and can realize novel sensing functions [1–6]. For very small diameter ($<$10 nm) wires, direct size effects on the electronic structure and the indirect effect of greater elastic compliance and its potential to avoid dislocation-mediated strain relaxation in core/shell nanowires offer additional means of engineering the properties of nano-scale semiconductors. Such structures can improve the performance of nanoelectronic devices by increasing conductivity through strain-induced mobility enhancements [7, 8] and creating band offsets to spatially separate carriers from scattering centers such as surface states and ionized dopants [9–11]. In nanophotonic devices, confining carriers away from the surface can increase emission efficiency [12], and the band gap can be tailored through strain effects [12, 13] and quantum confinement [14, 15]. Individual nanowires [16] and arrays of nanowires [17, 18] have enhanced absorption at certain frequencies, and the diameter, pitch, length and tapering can be specifically engineered for various optoelectronic applications. In order to realize their potential, however, a much more systematic understanding of nanowire growth and surface passivation are required.

This paper will summarize recent results from our group on low-temperature vapor–liquid–solid epitaxial growth of vertical Ge nanowires on Si and Ge substrates, on Ge-core/Si shell nanowire synthesis, and nanowire-seeded crystallization of amorphous semiconductor thin films. Epitaxy is investigated as a means of (1) directing nanowire growth, (2) controlling strain in Ge core-Si shell radial heterostructures and (3) producing large-area single-crystal Ge layers above a Si wafer surface.

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2. Low-temperature nanowire deposition and core-shell synthesis

The Ge NWs examined in our research were grown using colloidal gold particles of 10–40 nm diameter to catalyze local Ge growth during chemical vapor deposition (CVD). Substrates were Ge (1 1 1), Ge (0 0 1), Ge (1 1 0) and Si (1 1 1) single-crystal wafers. Detailed cleaning and surface preparation procedures for the Ge substrates both prior to colloidal gold coating and for spin coating of Au catalysts onto the germanium wafers prior to CVD are reported elsewhere [19–21]. Spin coating was used to produce a sparse distribution of Au catalysts and, therefore, of nanowires on the wafers, to simplify analysis of their morphology and crystallographic orientation after growth. Catalyst deposition by dip coating generally resulted in rather dense nanowire arrays (1–10 NW μm^{-2}). In Au catalyst deposition onto Si (1 1 1) substrates, a HF-acidified solution was first deposited onto the substrate surface [22] to prevent local oxidation of silicon in the vicinity of the catalysts. Nanowire growth was carried out in a cold-wall, lamp-heated, chemical vapor deposition chamber with GeH_4 precursor flow and H_2 carrier gas at a total pressure of 30 torr. In studies of Ge NW orientation selection on different Ge single-crystal substrates, a single substrate temperature of 350 °C was employed throughout the NW growth process [19]. This temperature is close to the bulk Au–Ge eutectic of 361 °C. In other experiments, a two-step thermal profile was used in which nanowires were nucleated at an elevated temperature (370–400 °C) and then most of the NW growth occurred during a longer steady-state growth step at a temperature in the range 280–300 °C [20, 21]. The CVD reactor uses halogen lamps to heat a 'susceptor stack' on which the substrates sit during deposition. Samples of germanium or Si wafer pieces are placed on a dummy silicon wafer, which rests on a silicon carbide susceptor, which in turn rests on another silicon wafer with an attached thermocouple. The substrate temperature is measured using the C-type thermocouple welded to a silicon wafer on the bottom of the susceptor stack. Radiative heating from the halogen bulbs allows for rapid thermal processing, in which the substrates can be heated from room temperature to the deposition set point temperature or from one set point to another in tens of seconds, and this procedure was performed during the two-step growth experiments.

In Ge core/Si shell coaxial nanowire synthesis, Ge NWs were deposited on Si (1 1 1) substrates using two-step growth (2 min nucleation at 375 °C/18 min growth step at 300 °C) followed by deposition of a conformal Si shell using a SiH_4/H_2 process at temperatures between 550 °C and 600 °C [23]. In some cases, a selective, iodide-based, etch [22] was used to remove the Au catalyst nanoparticles from the tips of the as-grown Ge nanowire cores prior to Si shell deposition. HCl flow was maintained, along with the SiH_4 and H_2 flow, during some of the shell depositions in order to suppress stress-driven roughening of the Si shells.

3. Results and discussion

3.1. Vapor–liquid–solid nanowire growth guided by epitaxy

Silicon and germanium nanowires deposited by Au-catalyzed CVD typically grow by the vapor–liquid–solid (VLS) mechanism [24], in which fcc Au particles melt and become supersaturated with Si or Ge, which precipitates out to form a single-crystal wire. The precursor CVD reaction is catalyzed locally at the Au surface, and the balance of surface tensions acting on the resulting Au–Ge liquid droplet and the NW growth facet is such that the droplet remains suspended at the tip of the growing NW and is translated through the gas phase as the wire lengthens. Ideally, the wire diameter is determined by the Au nanoparticle catalyst diameter and its location on the substrate by the initial location of the nanoparticle. Its length is determined by the rate of crystal growth via the VLS mechanism for the precursor, temperature and pressure conditions and, in some cases [25], the wire diameter.

We have studied the low-temperature, Au-catalyzed growth of Ge nanowire (NW) arrays synthesized via homoepitaxy on Ge substrates and by heteroepitaxy on Si substrates, as a means of preparing high-quality oriented arrays of single-crystal nanowires in a deterministic fashion. By using a two-temperature growth process in a rapid thermal CVD reactor, one can optimize NW nucleation and growth separately and thus increase wire yield while maintaining NW diameter control. Facile nucleation of Ge NWs with orientations that are dictated by an underlying Ge or Si substrate is found to occur at temperatures near the bulk eutectic [21]. However, at this temperature, growth in a relatively clean (low oxidant activity) CVD environment produces highly tapered nanowires, as depicted in figure 1. This occurs because the GeH_4 precursor decomposes readily on the Ge NW sidewall facets at this temperature, competing with its catalyzed decomposition on the Au–Ge nanoparticle tip. The base of a wire will, therefore, be coated by a much thicker layer of Ge than will the region near the NW tip, producing the taper evident in figure 1. The tapering observed in figure 1 does not appear to result from surface diffusion of Au along the growing nanowires. Hannon and co-workers [26] have reported both tapering (small tip, wide base) and inverse tapering (wide tip, smaller base) for Si NWs grown at higher temperatures *in situ* in a TEM, and have shown that these results from coarsening of the Au–Si droplets during VLS growth. We do not observe inverse tapering during Au-catalyzed Ge NW growth (at much lower temperatures than those used by Hannon *et al*), nor does growth appear to cease for our nanowires as a result of the disappearance of the Au from the tips of smaller diameter wires. Both observations would be expected for the Au coarsening mechanism, but are not found in our experiments.

Figure 1 shows Ge NWs deposited onto a Ge (1 1 1) substrate. Essentially all of the nanowires observed exhibit an epitaxial relationship with the underlying single-crystal substrate. These wires, which nucleated from colloidal Au catalyst particles with a nominal diameter of 10 nm, grow along either the vertical or inclined Ge ⟨1 1 1⟩ crystallographic axes, with most of the NWs being vertical. The ⟨1 1 1⟩ growth

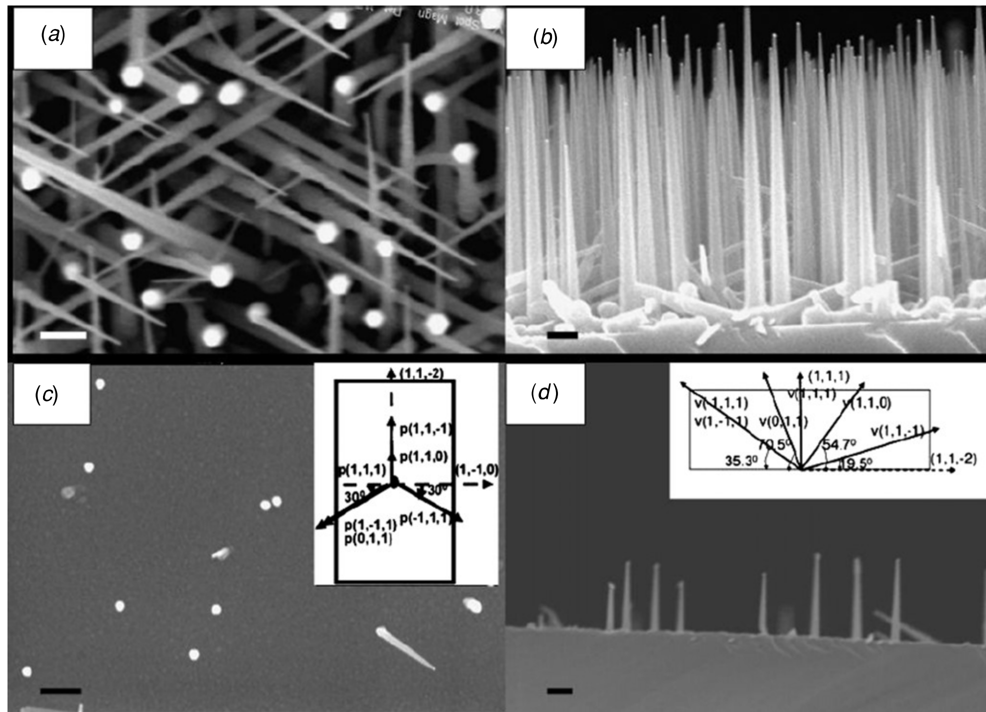


Figure 1. (*a*) Plan view and (*b*) vertical view SEM image of GeNWs grown on the Ge (1 1 1) substrate with dense gold colloids. (*c*) Plan view and (*d*) vertical view SEM image of GeNWs grown on the Ge (1 1 1) substrate with scattered gold colloids. The inset represents schematically the projections of nanowires growing along various growth directions viewed (*c*) along substrate normal, represented by *p*(growth direction) and (*d*) perpendicular to substrate normal, represented by *v*(growth direction). All the nanowires are growing along ⟨1 1 1⟩ directions. All scale bars are 200 nm [19].

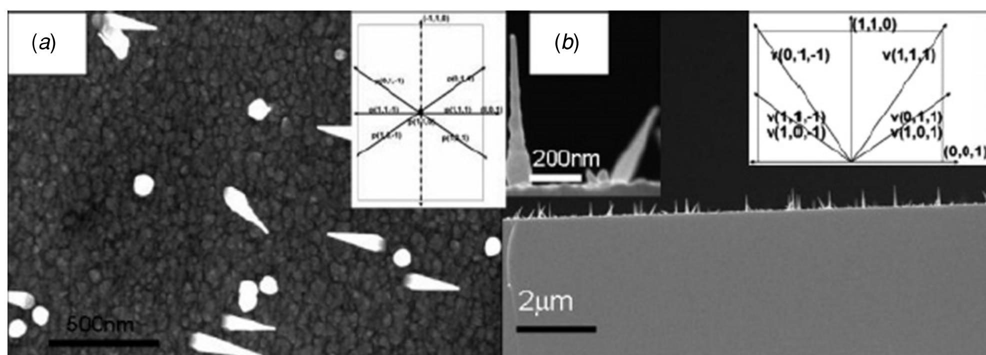


Figure 2. (*a*) Plan view and (*b*) vertical view SEM image of GeNWs grown on the Ge (1 1 0) substrate with scattered gold colloids. Inset shows the schematic projections of nanowires growing along various growth directions viewed (*a*) along substrate normal, represented by *p*(growth direction) and (*b*) perpendicular to substrate normal, represented by *v*(growth direction). Nanowire growth is along the ⟨1 1 0⟩ and ⟨1 1 1⟩ directions [19].

directions were also observed for nanowires deposited using the same Au colloids under identical growth conditions on Ge (1 0 0) and Ge (1 1 0) single-crystal substrates; however, wires growing along ⟨1 1 0⟩ axes (also epitaxial with the substrate) were also present. Figure 2 shows a typical arrangement of wires on the Ge (1 1 0) substrate, indicating the preference for ⟨1 1 0⟩ growth on this substrate. The results shown in figures 1 and 2 indicate the extent to which epitaxy can influence nanowire growth directions during vapor–liquid–solid NW synthesis.

In addition to epitaxy on a single-crystal substrate, which governs the morphology of the NW during its nucleation and initial stages of growth, NW orientation selection can result from a competition between surface and interface energy terms arising from the liquid droplet/NW growth facet contact near the wire tip as the wire grows. This situation has been analyzed theoretically by Schmidt and co-workers for the case of VLS growth of Si NWs using Au nanoparticle catalysts [27]. Considering the wire-radius scaling of the energy of the Si wire surface, the NP/NW interface along the growth facet and the line tension at the triple-phase-boundary (vapor, liquid, solid) surrounding the growth facet, these authors showed that a transition from a ⟨1 1 0⟩ to a ⟨1 1 1⟩ growth direction was expected for nanowires with a radius exceeding some critical value (approximately 20 nm), consistent with their experimental results. We have observed

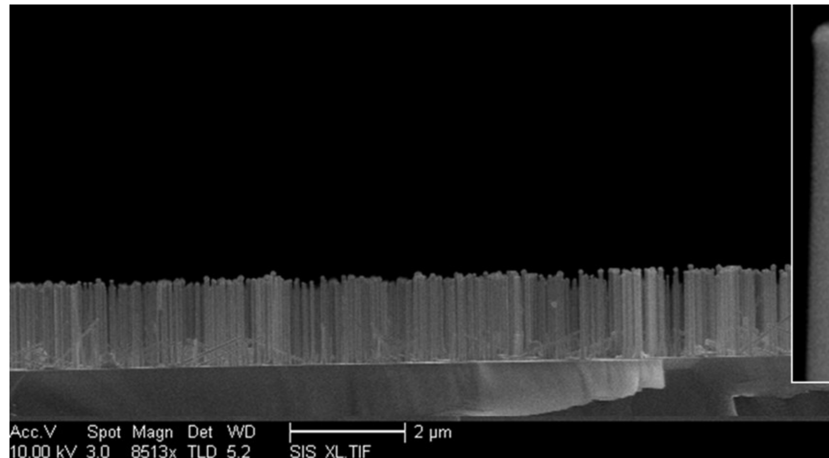


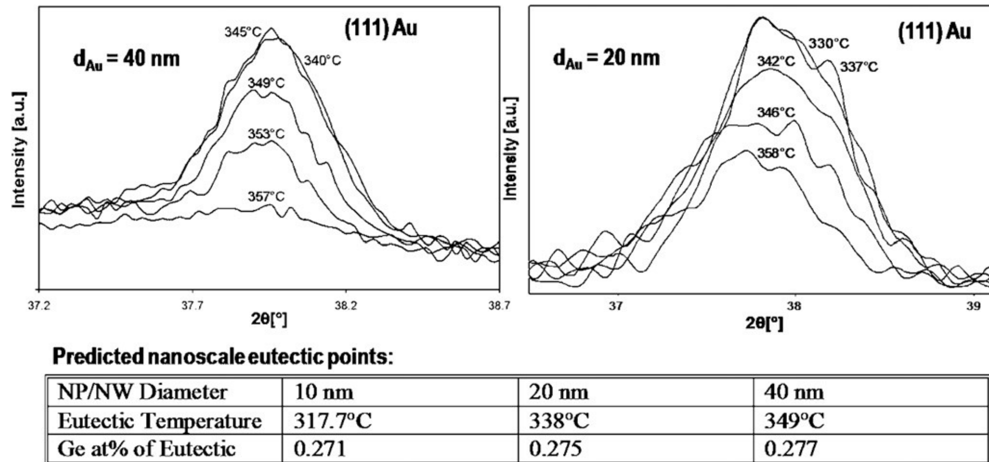
Figure 3. Dense array of untapered, ⟨1 1 1⟩-oriented Ge NWs deposited on a (1 1 1) Ge single-crystal substrate by Au-catalyzed CVD with GeH_4/H_2 using a two-temperature deposition process: 2 min at 400 °C and 18 min at 280 °C. In addition to the dominant vertical [1 1 1]-oriented wires, a smaller fraction of the NWs grow along the inclined ⟨1 1 1⟩ axes [19].

a similar NW radius dependence for ⟨1 1 1⟩ Ge NW growth when the wires are grown using a process that inhibits tapering (described below). However, for the tapered NWs shown in figures 1 and 2, the axial wire orientation appears to be most affected by the crystallographic orientation of the underlying substrate (presumably, a nucleation effect). This may be a consequence of the grown-in taper for these wires, which will alter the balance of capillary forces acting on the NW/NP interface [28, 29].

By adopting the aforementioned two-temperature step process [19, 30], wires that were almost taper-free over most of their length were deposited. A representative image is shown in figure 3. Most of the NW growth took place during the low temperature (280–300 °C) step, during which sidewall decomposition of the GeH_4 precursor molecules was, apparently, kinetically inhibited. By confining GeH_4 decomposition to the vicinity of the Au–Ge catalyst droplet, all Ge added to wire is incorporated at the growth facet, producing one-dimensional crystal growth. Kodambaka *et al* [31] have also reported taper-free Si NW growth, by intentional incorporation of oxygen into the CVD growth environment. Oxygen exposure of the surfaces of the NW sidewalls was found to inhibit Au surface diffusion in their (higher temperature, 600–650 °C) growth experiments, and thus it avoids the coarsening mechanism for nanowire tapering reported by Hannon *et al*. In addition to blocking Au surface diffusion, adsorbed oxygen may inhibit non-catalyzed precursor decomposition and adatom diffusion on nanowire sidewalls. The effects of such surface-active species on the morphological stability of strain core/shell nanowires will be discussed elsewhere in this paper.

By achieving a sudden change in temperature after the initiation of nanowire CVD, our rapid thermal growth reactor made possible a substantial reduction in the Ge NW taper. In addition, this capability permits NW nucleation and growth to be decoupled for detailed kinetic studies [20, 21]. Analysis of the time dependence of average nanowire length in both single-step and two-step growth at various temperatures indicates that Ge NW growth in our system has a relatively weak temperature dependence. Approximately 90% of the wire length observed in figure 3 formed during the low temperature step at deep subeutectic temperatures at a growth rate comparable to that during the 'nucleation step' at 400 °C. The fact that the wire growth rate is not strongly affected by the sudden (<60 s cooling duration) temperature decrease between the steps and that the crystalline orientation and wire morphology were preserved throughout wire growth suggests no sudden change in the wire growth mechanism. Therefore, consistent with the *in situ* TEM observations reported by Kodambaka *et al* using a digermane precursor at much lower pressures [32], we conclude that VLS can occur in the deep subeutectic temperature regime for the Au–Ge system. As shown in figure 3, steady-state growth of Ge NWs can be achieved at temperatures (280–300 °C) far below the bulk Au–Ge eutectic point (361 °C) after wires nucleate at a temperature near or above the eutectic. One possible explanation for this effect is a capillary lowering of the Au–Ge eutectic temperature in this nano-scale system compared to the reported bulk three-phase (face centered cubic Au–Ge solid solution, liquid and Ge) equilibrium. We have analyzed this hypothesis [20] both theoretically [33], by considering the effects of Gibbs–Thomson pressure terms on the free energies of the various phases (including the impact of surface adsorption of Ge on the Au–Ge liquid surface energy), and experimentally, by measuring the melting point of Au catalyst nanoparticles at the tips of VLS-grown Ge NWs of various diameters (figure 4). The results obtained in these experiments indicate that size effects do tend to suppress the eutectic temperature in the NP/NW Au–Ge system; however, the temperature reduction is too small to account for the observed two-step VLS growth behavior for the range of Au catalyst diameters that we have investigated.

Instead, as was proposed by Kodambaka *et al* [32], our observations indicate that a significant kinetic barrier to Au catalyst solidification exists during VLS growth of Ge NWs. Two phenomena contribute to the metastability of the liquid phase: the barrier to (likely homogeneous) nucleation of solid Au in the nano-scale Au–Ge liquid droplet [20, 33] and the



NP/NW Diameter	10 nm	20 nm	40 nm
Eutectic Temperature	317.7°C	338°C	349°C
Ge at% of Eutectic	0.271	0.275	0.277

Figure 4. Top panels: measured intensity of the Au (1 1 1) x-ray diffraction peak (symmetric scans, Cu-K_α radiation) measured during slow-heating of Ge NWs with Au catalyst tips of 40 nm and 20 nm nominal diameter; note the reduction in the apparent Au–Ge eutectic melting temperature compared to the bulk eutectic (361 °C) and the trend of decreasing eutectic temperature with Au catalyst diameter. Lower panel: table listing the calculated capillary lowering of the eutectic temperature and Ge composition for several different Au catalyst nanoparticle (NP) diameters [20].

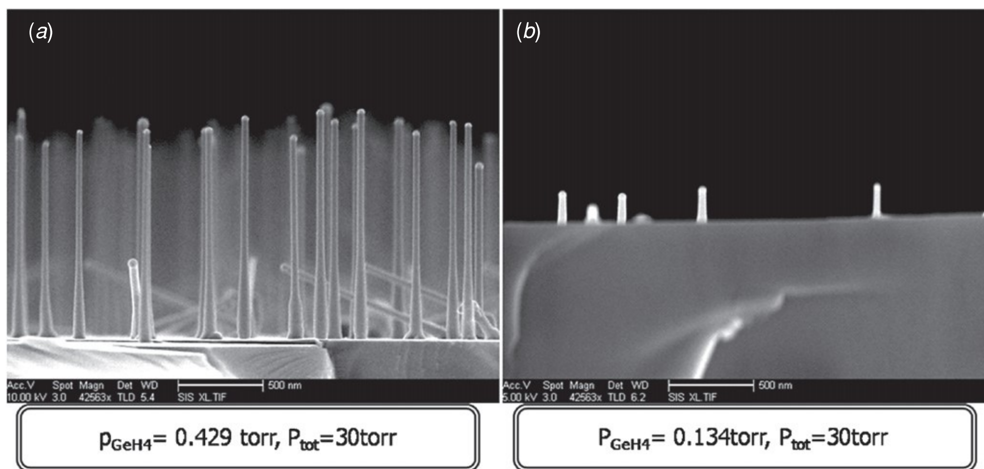


Figure 5. Two-temperature step deposition (100 s/400 °C, 10 min/280 °C) results for (*a*) standard germane partial pressure in H_2 carrier gas and (*b*) reduced germane partial pressure. Under the conditions in (*a*), steady-state nanowire growth occurs at 280 °C, whereas NW growth is suppressed at this deep subeutectic temperature in the less germane-rich CVD environment of (*b*) [21].

super-saturation of the liquid catalyst with Ge during CVD growth [20, 21, 32]. The latter effect can be investigated by varying the germane partial pressure in the GeH_4/H_2 NW CVD environment. Under our standard growth conditions, where $P(GeH_4) = 0.429$ torr, the lowest temperature at which steady-state NW growth can be sustained during the second, lower temperature, step of the two-step process is 280 °C (figure 5(*a*)). Reducing $P(GeH_4)$ to 0.134 torr for the same two-step temperature profile produced nucleation of the nanowires and their initial growth during the higher temperature step (figure 5(*b*)), but minimal extension of the wires at 280 °C. Increasing $P(GeH_4)$ in the CVD reactor to 1.034 torr reduced the minimum temperature at which steady-state growth of the Ge NWs occurred to 250 °C. These results are consistent with stabilization of the Au–Ge liquid to lower temperatures as the concentration of Ge dissolved in the liquid is forced to larger values during wire deposition. The increase in the Ge content in the liquid reduces the chemical potential of Au, removing the driving force for its solidification even at very low temperatures [20, 21]. The lower Ge content produced in the liquid under the deposition conditions depicted in figure 5(*b*) leads to solidification of the Au–Ge droplet during cooling to 280 °C, greatly reducing the rate of NW growth [32].

Interestingly, deep subeutectic VLS growth has not, to our knowledge, been reported for Si NW deposition, despite the similar thermodynamics of the Au–Ge and Au–Si binary systems. This may result from differences in precursor reactivity between Si and Ge CVD precursors at low temperatures, but the precise mechanisms responsible for this difference require further investigation.

3.2. Epitaxial core-shell nanowires

Radially heterostructured Group IV nanowires can significantly improve the performance of nanoelectronic devices and

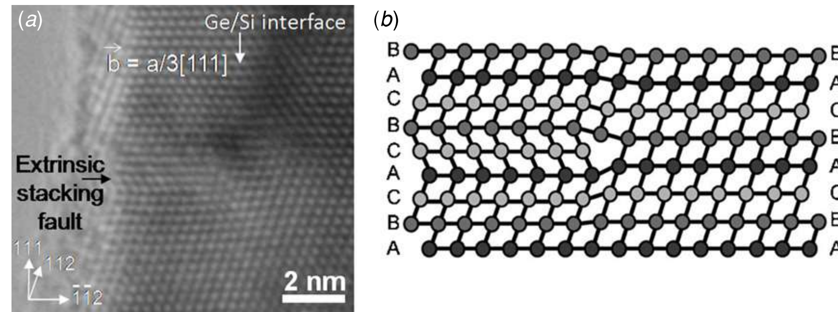


Figure 6. (*a*) TEM image of a loop dislocation with $\mathbf{b} = a/3[1\,1\,1]$ in a 28 nm Ge-core/4.5 nm Si-shell nanowire that produces an extrinsic stacking fault in the shell; (*b*) schematic showing atomic column positions in the vicinity of the stacking fault [23].

enable new device architectures [34, 35]. In particular, epitaxial strain and quantum confinement in core-shell nanowires effects may allow the engineering of unique photonic and electronic properties. However, this same epitaxial strain induced by the large lattice mismatch between heteroepitaxial Si shells around Ge nanowires induces roughening of the shell surface [36, 37], creating regions of high stress concentration in the shell where misfit dislocations can nucleate (figure 6) [23].

In our experiments, gold-catalyzed, chemical vapor-deposited Ge nanowires were first synthesized, followed by the heteroepitaxial deposition of a SiGe shell using silane and germane. Axial and radial components of strain in the core/shell structures were measured by x-ray diffraction from epitaxial nanowire arrays to probe the strain relaxation processes quantitatively, and these data were compared with the densities of dislocations observed by transmission electron microscopy. Stress relaxation via either surface roughening or dislocations is encouraged by structures in which the Ge core is relatively thick, and therefore, non-compliant, elastically. The results of detailed electron microscopy and high-resolution x-ray diffraction studies [23] indicate that (1) dislocations form preferentially at regions of concave surface curvature on the shell surface; (2) the majority of dislocations are prismatic (1 1 1) loops that relieve axial strains between the Ge core (in compression) and the Si shell (in tension); and (3) circumferential and radial components of strain in the Ge core are, compared to axial strains, relatively unrelaxed in dislocated core/shell wires.

By inhibiting surface roughening of a Si or Si-rich SiGe shell, dislocation formation is prevented and coherent structures can be obtained (figure 7). Recent work has demonstrated [38] that strain-driven shell roughening on ⟨1 1 1⟩-oriented core/shell wires can be avoided by flowing HCl during SiH_4/H_2 CVD of the shell. Although the etch rate of Si at the temperatures used for shell growth (550–600 °C) is expected to be small, it is possible that asperities may be removed from the shell surface before they can grow. Alternatively, HCl exposure should result in transient Cl bonding to the Si surface, and this may inhibit Si adatom surface diffusion that is required for amplification of Si shell roughness. Moreover, reducing the Ge core radius can inhibit roughening, a result of both the increasing elastic compliance of the core and of a transition to a different crystallographic orientation during Ge NW growth. Epitaxial Ge NWs with a diameter of ∼10 nm or less grow preferentially in a ⟨1 1 0⟩ crystallographic orientation on Si (1 1 1) substrates. Wires of this orientation are bounded by low-energy {1 1 1} and {1 0 0} facet planes which are more resistant to roughening than the facet planes surrounding ⟨1 1 1⟩-oriented nanowires. By controlling the Si shell thickness and Ge core radius, it is possible to achieve fully coherent Si-shell/Ge-core nanowires of lengths exceeding 1 μm.

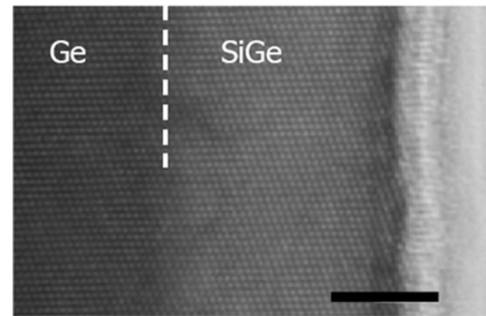


Figure 7. TEM cross-section image along the ⟨1 1 0⟩ zone axis of a ⟨1 1 1⟩-oriented core-shell nanowire in which the $Si_{0.25}Ge_{0.75}$ shell was deposited in flowing SiH_4/HCl with H_2 carrier gas. Scale bar is 5 nm [38].

3.3. Vertical Ge NW seeds for liquid-phase epitaxy of large-area Ge islands on Si

Germanium layers heterogeneously integrated on silicon are interesting for transistor applications because germanium has large intrinsic electron and hole mobilities [39]. Recent work on surface passivation of planar germanium surfaces with high-dielectric-constant materials [40, 41] makes possible the fabrication of high-mobility, Ge-channel metal-oxide-semiconductor (MOS) devices, prompting interest in integration of Ge single-crystal layers in Si-based semiconductor circuits. There is also great interest in Ge integration on Si substrates to enable on-chip optoelectronics. Finally, germanium has good lattice matching with III–V semiconductors (e.g. GaAs), and it can, therefore, be used as a buffer layer for integration of III–V materials on Si.

Recently, we have investigated the use of epitaxial Ge ⟨1 1 1⟩ nanowires as seeds for the crystallization of initially amorphous Ge layers deposited on Si substrates coated with

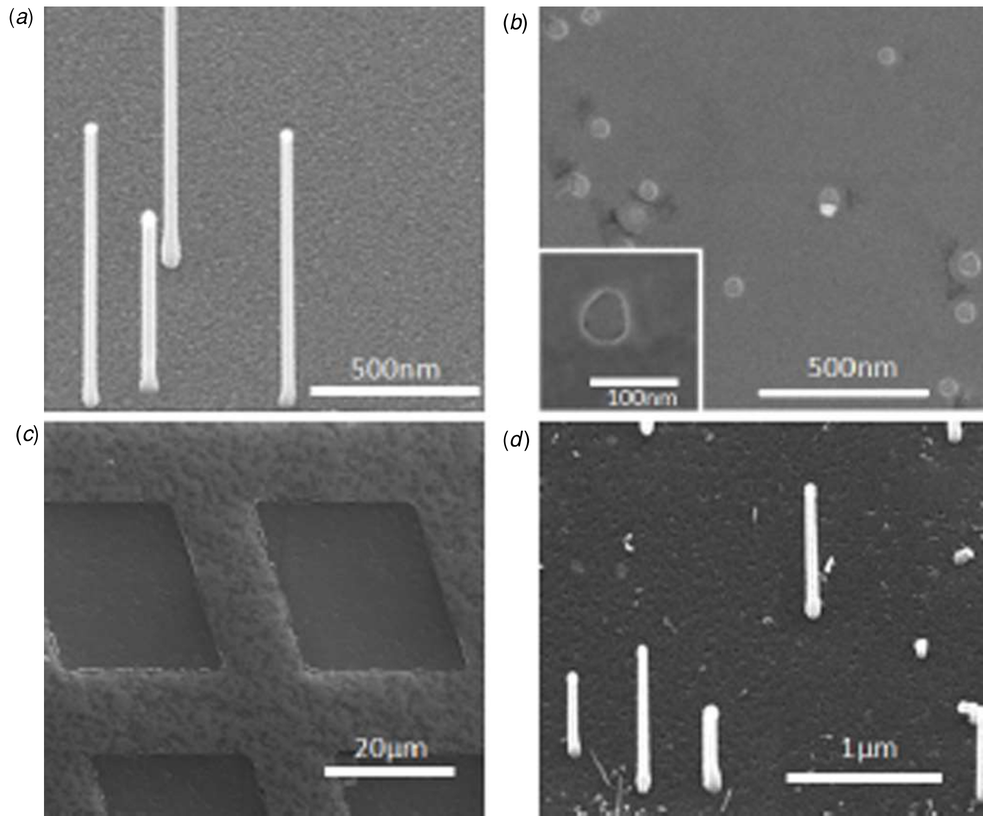


Figure 8. SEM micrographs of the samples at various points in the processing sequence. (*a*) 45° from the plan-view image of germanium nanowires on a (1 1 1) silicon substrate. (*b*) Plan-view SEM image of as-exposed germanium nanowire tips after the CMP process. The inset shows the top view of one polished nanowire. (*c*) 45° from the plan-view image of germanium islands before annealing. (*d*) 45° from the plan-view image of epitaxial germanium nanowires grown on one crystallized germanium island [44].

planarized and thick SiO_2 films. This approach, which builds on the previous work on seeded liquid-phase epitaxy (LPE) of Ge crystals [42, 43], uses single-crystal Ge NWs to transmit the crystalline orientation and perfection of the Si substrate to overlying Ge layers that can be located microns above the level of MOS devices on the Si wafer [44]. Moreover, the single-crystal Ge layers can themselves then act as templates for subsequent vertical Ge NW growth (figure 8), allowing the potential application of this method for multiple active layers in 3D integrated circuits.

As shown in figure 8(*a*), vertical Ge NWs are grown by Au-catalyzed VLS chemical vapor deposition on a Si (1 1 1) substrate. These are coated by SiO_2 using a low-temperature, plasma-enhanced CVD process, and then the coated NW array is planarized by chemical mechanical planarization (CMP), exposing the polished cross-sections of the Ge NW single crystals (figure 8(*b*) and inset). Deposition of an amorphous Ge (*a*-Ge) film and its patterning into large islands (figure 8(*c*)) on the planarized oxide-coated NW layer produces test structures for Ge single-crystal growth above the Si (1 1 1) substrate surface. Rapid thermal annealing of the samples to a temperature slightly greater than the melting point of bulk Ge is used to melt the amorphous Ge islands, which crystallize during subsequent cooling during which the underlying Ge NWs in contact with each island act as seeds for *a*-Ge crystallization. Instead of rapid thermal annealing, pulsed laser annealing could also be used to melt the *a*-Ge islands, with less heat transfer to possible device structures on the underlying Si substrate. Nanowire-seeded LPE of the Ge islands during cooling after the rapid thermal anneal results in the formation of large-area single-crystal islands which can then act as substrates for subsequent Au-catalyzed VLS growth of a second epitaxial Ge NW array, as shown in figure 8(*d*).

For seeded crystallization to grow large-area single-crystal films from an initially liquid or amorphous state, there are two requirements: during the thermal process, any emerging or existing poly-Ge grains are eliminated by transient melting (for example, LPE), and the seeded crystallization happens in a temperature window where the growth front propagates sufficiently quickly to occlude unseeded nucleation sites in the region of interest. The rapid thermal anneal (RTA) temperature for successful LPE growth, 940 °C, is similar to the melting point of bulk crystalline germanium. As the temperature decreases rapidly at the end of the RTA (at a rate of 100 ks^{-1}), epitaxial growth of crystalline-Ge (*c*-Ge) seeded by the nanowires occurs as the *c*-Ge/liquid-Ge (*l*-Ge) interface sweeps across the undercooled *l*-Ge layer. Single-crystal Ge layers with the 30 μm × 30 μm area can be grown by this method [44].

4. Summary

Many technological applications of semiconductor nanowires require control of their crystallographic orientation and of

their direction of growth with respect to a large-area substrate. Such control can be achieved by metal nanoparticle catalyzed, vapor–liquid–solid, NW growth on lattice-matched substrates. However, the orientation selection imparted by epitaxy must, in some cases, compete with capillary effects that also tend to guide nanowire growth along certain crystallographic axes. In the case of epitaxial growth of untapered Ge NWs on Ge and Si single-crystal substrates, we find that, similar to reports for Si NW growth [27, 45], orientation selection is strongly influenced by the initial catalyst diameter. In the case of tapered nanowires, in which uncatalyzed decomposition of GeH_4 occurs on the wire sidewall facets during growth, capillary effects appear to be less effective in dictating the growth axes of nanowires grown on lattice-matched substrates compared to the templating effect of the underlying substrate.

Epitaxy between misfitting core and shell materials in coaxial nanowire heterostructures produces stress-driven roughening [46] and misfit dislocation formation [47] analogous to planar thin film heterostructures. However, the small radial and circumferential dimensions of untapered nanowires allow those strain components to be accommodated elastically in many cases, whereas axial strains are more readily relaxed inelastically. We have found that axial strains are effectively relieved by prismatic (1 1 1) dislocation loops at the interface between Si shells and Ge cores in ⟨1 1 1⟩-oriented core/shell NWs. These loops appear to nucleate preferentially at locations of concave curvature on the shell surface at which the tensile misfit strain in the Si shell is concentrated. By inhibiting shell roughening during its growth, fully coherent core/shell wires in the Si–Ge system can be synthesized using VLS-grown Ge nanowires coated by Si or SiGe epilayers deposited in a conformal CVD process.

Acknowledgments

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