LETTER

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Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors

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Over the past several years, the inherent scaling limitations of silicon (Si) electron devices have fuelled the exploration of alternative semiconductors, with high carrier mobility, to further enhance device performance[1–8]. In particular, compound semiconductors heterogeneously integrated on Si substrates have been actively studied[7,9,10]: such devices combine the high mobility of III–V semiconductors and the well established, low-cost processing of Si technology. This integration, however, presents significant challenges. Conventionally, heteroepitaxial growth of complex multilayers on Si has been explored[9,11–13]—but besides complexity, high defect densities and junction leakage currents present limitations in this approach. Motivated by this challenge, here we use an epitaxial transfer method for the integration of ultrathin layers of single-crystal InAs on Si/SiO_2 substrates. As a parallel with silicon-on-insulator (SOI) technology[14], we use 'XOI' to represent our compound semiconductor-on-insulator platform. Through experiments and simulation, the electrical properties of InAs XOI transistors are explored, elucidating the critical role of quantum confinement in the transport properties of ultrathin XOI layers. Importantly, a high-quality InAs/dielectric interface is obtained by the use of a novel thermally grown interfacial $InAsO_x$ layer (~1 nm thick). The fabricated field-effect transistors exhibit a peak transconductance of ~1.6 mS μm^{-1} at a drain–source voltage of 0.5 V, with an on/off current ratio of greater than 10,000.

Epitaxial lift-off and transfer of crystalline microstructures to various support substrates has been shown to be a versatile technique for applications ranging from optoelectronics to large-area electronics[15–18]. Specifically, high-performance, mechanically flexible macro-electronics and photovoltaics have been demonstrated on plastic, rubber and glass substrates by this method[19–21]. Here we use a modified epitaxial transfer scheme for integrating ultrathin InAs layers (with nanometre-scale thicknesses) on Si/SiO_2 substrates for use as high-performance nanoscale transistors. These InAs layers are fully depleted, which is an important criterion for achieving high-performance field-effect transistors (FETs) with respectable 'off' currents based on small bandgap semiconductors. The transfer is achieved without the use of adhesive layers, thereby allowing the use of purely inorganic interfaces with low interface trap densities and high stability. Figure 1a shows a diagram of the fabrication process for InAs XOI substrates (see Methods for details).

We used atomic force microscopy (AFM) to characterize the surface morphology and uniformity of the fabricated XOI substrates. Figure 1b and c shows representative AFM images of an array of InAs nanoribbons (~18 nm thick) on a Si/SiO_2 substrate, clearly depicting the smooth surfaces (<1 nm surface roughness) and high uniformity of the enabled structures over large areas. Uniquely, the process readily enables the heterogeneous integration of different III–V materials and structures on a single substrate through a multi-step epitaxial transfer process. To demonstrate this capability, a two-step transfer process was used to form ordered arrays of 18- and 48-nm-thick InAs nanoribbons that are perpendicularly oriented on the surface of a Si/SiO_2 substrate (Fig. 1d, e). This result demonstrates the potential capacity of the proposed XOI technology for generic heterogeneous and/or hierarchical assembly of crystalline semiconducting materials. In the future, a similar scheme may be used to enable the fabrication of both p- and n- type transistors on the same chip for complementary electronics based on the optimal III–V semiconductors.

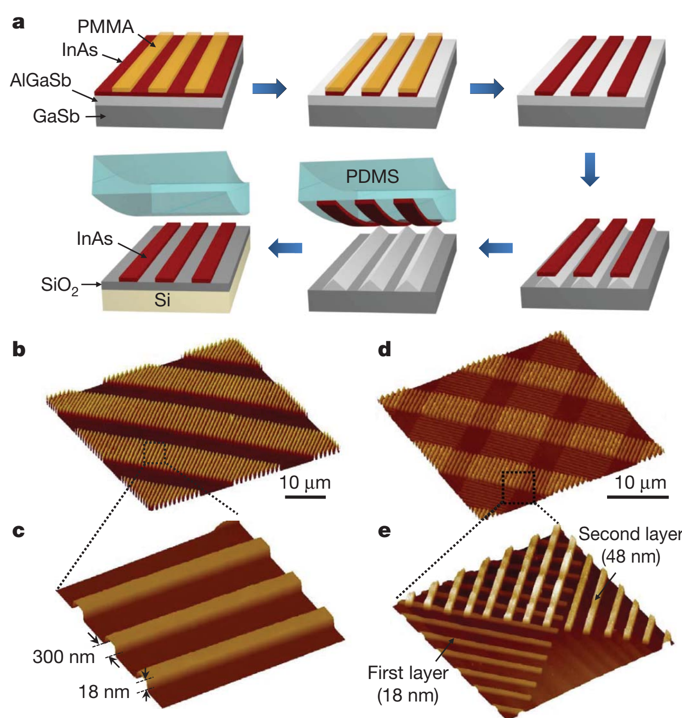

Figure 1 | Fabrication scheme for ultrathin InAs XOI, and AFM images. **a**, Schematic procedure for the assembly of InAs XOI substrates by an epitaxial transfer process. The epitaxially grown, single-crystal InAs films are patterned with PMMA and wet etched into nanoribbon arrays. A subsequent selective wet etch of the underlying AlGaSb layer and the transfer of nanoribbons by using an elastomeric PDMS slab result in the formation of InAs nanoribbon arrays on Si/SiO_2 substrates. **b**, **c**, AFM images of InAs nanoribbon arrays on a Si/SiO_2 substrate. The nanoribbons are ~10 μm long, 18 nm high and ~300 nm wide. **d**, **e**, AFM images of InAs nanoribbon superstructures on a Si/SiO_2 substrate, consisting of two layers of perpendicularly oriented nanoribbon arrays with 18- and 48-nm thicknesses, as assembled by a two-step epitaxial transfer process.

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To shed light on the atomic structure of the interfaces, cross-sectional transmission electron microscopy (TEM) images of an InAs XOI device were taken and are shown in Fig. 2. The high-resolution TEM (HRTEM) image (Fig. 2c) illustrates the single-crystal structure of the InAs nanoribbons (~13 nm thick) with atomically abrupt interfaces with the SiO_2 and ZrO_2 layers. The TEM image of the InAs/SiO_2 interface does not exhibit visible voids (Fig. 2c), although only a small fraction of the interface is examined by TEM. As described in more depth below, InAs nanoribbons were thermally oxidized before the top-gate stack deposition to drastically lower the interfacial trap densities. The thermally grown $InAsO_x$ layer is clearly evident in the HRTEM image (Fig. 2c), with a thickness of ~1 nm.

Long-channel, back-gated FETs based on individual nanoribbons were fabricated in order to elucidate the intrinsic electron transport properties of InAs nanoribbons as a function of thickness. The process scheme involved the fabrication of XOI substrates with the desired InAs thickness, followed by the formation of source/drain (S/D) metal contacts by lithography and lift-off (~50-nm-thick Ni). The p^+ Si support substrate was used as the global back-gate, with a 50-nm thermal SiO_2 layer as the gate dielectric. Nickel contacts were annealed at 225 °C for 5 min in N_2 to enable the formation of low-resistance contacts to the conduction band of InAs (Supplementary Fig. 6)[22]. The transfer characteristics (at a drain–source voltage (V_{DS}) of 0.1 V) of the back-gated XOI FETs with a channel length $L \approx 5\ \mu m$ and InAs thicknesses of 8–48 nm are shown in Fig. 3a. Two trends are clearly evident from the measurements. First, the 'off' current monotonically increases with increasing thickness, owing to the reduced electrostatic gate coupling of the back-gate. Second, the 'on' current increases with InAs thickness, owing to the thickness dependence of electron mobility, μ_n. As $L \approx 5\ \mu m$, the devices are effectively operating in the diffusive regime, thereby enabling the direct extraction of the field-effect mobility ($\mu_{n,FE}$) by using the relation $\mu_{n,FE} = g_m(L^2/C_{ox}V_{DS})$, where $g_m = dI_{DS}/dV_{GS}|_{V_{DS}}$ is the transconductance, C_{ox} is the gate oxide capacitance, I_{DS} is drain–source current and V_{GS} is gate–source voltage (Supplementary Fig. 5). For this analysis, parasitic resistances were ignored because Ni forms near-ohmic metal contacts[22]. The gate oxide capacitance was estimated from the parallel plate capacitor model $C_{ox} = (\varepsilon A)/d$, where $\varepsilon = 3.9$ and $d = 50$ nm are the dielectric constant and thickness of SiO_2, respectively. The effect of quantum capacitance, C_Q, was neglected owing to the relatively thick gate dielectrics used in this study (that is, $C_{ox} \ll C_Q$). Figure 3b shows the peak $\mu_{n,FE}$ as a function of InAs thickness, T_{InAs}. The mobility at first linearly increases with thickness for $T_{InAs} < \sim 18$ nm with a slope of $\sim 221\ cm^2\,V^{-1}\,s^{-1}\,nm^{-1}$, beyond which it nearly saturates at $\mu_{n,FE} \approx 5{,}500\ cm^2\,V^{-1}\,s^{-1}$. The measured XOI field-effect mobility is close to the reported Hall mobilities for InGaAs ($\sim 10{,}000\ cm^2\,V^{-1}\,s^{-1}$)[10] and InAs ($13{,}200\ cm^2\,V^{-1}\,s^{-1}$)[23] quantum well structures. It should be noted that the Hall mobility is typically higher than the field-effect mobility for any given material, as a number of device and surface state contributions to carrier transport are not accounted for in the Hall effect measurements.

To shed light on the observed mobility trend, the low-field phonon mobility, $\mu_{n,phonon}$, was calculated as $\mu_{n,phonon} = e/(m^*\langle 1/\tau \rangle)$, where e is the electronic charge, and m^* is the effective mass (Supplementary Information). Average scattering rate $\langle 1/\tau \rangle$ is calculated from

$$\langle 1/\tau \rangle = \frac{\int \frac{1}{\tau(E)} \frac{\partial f_0}{\partial E} dE}{\int \frac{\partial f_0}{\partial E} dE}$$

where f_0 is the equilibrium Fermi–Dirac distribution function. $\tau(E)$ was calculated using Fermi's golden rule, with the matrix elements of the scattering potentials evaluated in the basis of the nanoribbon eigenfunctions. Both acoustic and optical (including polar) phonon scattering events were considered[24]. The plot of calculated $\mu_{n,phonon}$ versus T_{InAs} is shown in Fig. 3b. For small thicknesses, the mobility increases linearly with the thickness. This behaviour is attributed to the gradual transition of the channel from a two-dimensional to a three-dimensional system as the nanoribbon thickness is increased, with more transport modes (that is, sub-bands) contributing to the current flow. As the thickness increases to a value greater than the Bohr radius of bulk InAs (~34 nm), the electronic structure of the nanoribbons approaches the three-dimensional regime, resulting in a mobility saturation (for $T_{InAs} > \sim 35$ nm) to the well-known bulk value of InAs ($\sim 40{,}000\ cm^2\,V^{-1}\,s^{-1}$)[25]. Whereas the thickness for the onset of saturation closely matches the experiments, there is a discrepancy of 5–10 times in the actual mobility values. This is expected, as the extracted data represent the field-effect mobility, consisting of phonon scattering along with other device contributions (including interface trap states, surface roughness scattering, and vertical-field-induced mobility degradation). Both surface roughness and vertical field (that is, gate field) induce additional carrier scattering events at the surface/interface, while the interface trap states cause the gate-channel coupling efficiency to deteriorate. These effects degrade the extracted g_m and thereby $\mu_{n,FE}$.

To simulate $\mu_{n,FE}$, a full device simulation was performed (Supplementary Information). Using an interface trap density, D_{it}, as the fitting parameter; we obtained $D_{it} = 6 \times 10^{12}$ states $cm^{-2}\,eV^{-1}$. The simulated current–voltage (I–V) characteristics of XOI back-gated FETs are shown in Fig. 3a. Clearly, the simulated I–V curves match the experimental data closely for all InAs thicknesses, especially in the on-state. Next, peak $\mu_{n,FE}$ was extracted from the simulation and

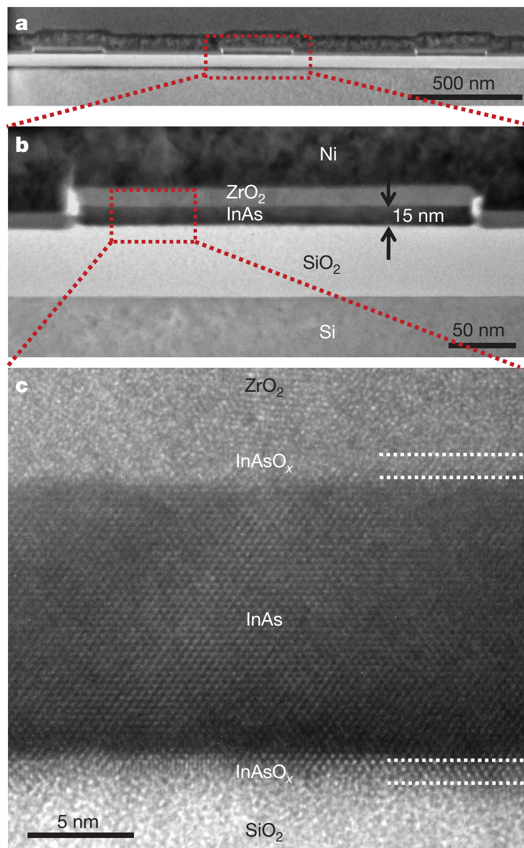

Figure 2 | Cross-sectional TEM analysis of InAs XOI substrates. **a**, TEM image of an array of three InAs nanoribbons on a Si/SiO_2 substrate. **b**, Magnified TEM image of an individual ~13-nm-thick InAs nanoribbon on a Si/SiO_2 (~50 nm thick) substrate. The nanoribbon is coated with a ZrO_2/Ni bilayer (~15 and ~50 nm, respectively), which acts as a top-gate stack for the subsequently fabricated FETs. **c**, HRTEM image showing the single-crystal structure of an InAs nanoribbon with abrupt atomic interfaces with ZrO_2 and SiO_2 layers on the top and bottom surfaces, respectively. An ~1-nm-thick $InAsO_x$ interfacial layer formed by thermal oxidation and used for surface passivation is clearly evident.

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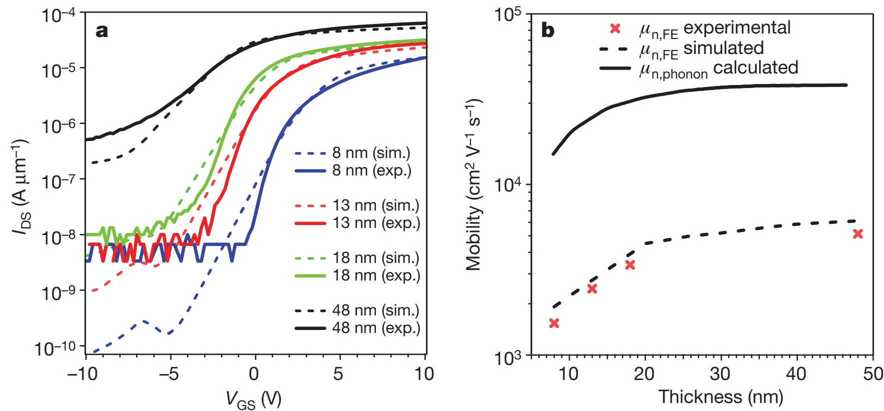

Figure 3 | Back-gated, long-channel InAs XOI FETs. a, Experimental (solid lines) and simulated (dashed lines) I_{DS}–V_{GS} characteristics of back-gated (50-nm SiO_2 gate dielectric) XOI FETs at $V_{DS} = 0.1$ V with $L \approx 5$ μm for different InAs nanoribbon thicknesses (8, 13, 18, 48 nm). Each FET consists of a single nanoribbon. **b**, Experimental and simulated peak field-effect electron mobilities ($\mu_{n,FE}$) of InAs nanoribbons as a function of nanoribbon thickness. The calculated phonon mobility ($\mu_{n,phonon}$) is also shown.

plotted as a function of T_{InAs} (Fig. 3b), once again closely matching the experimental $\mu_{n,FE}$. The close matching of the experimental and simulated results demonstrate the effectiveness of the XOI platform as a clean and predictable material system for exploring high-performance devices while highlighting the critical role of quantum confinement and surface contributions in the transport properties of InAs, even at relatively large thicknesses. It should be noted that since the ribbon width used in this work is 10–30 times larger than the thickness, there is minimal dependence of the device performance on nanoribbon width (Supplementary Fig. 13), so the structures can be effectively treated as thin films.

In order to explore the performance limits of InAs XOI devices, top-gated FETs with high-dielectric-constant (high-κ) gate insulators and $L \approx 0.5$ μm were fabricated. Briefly, Ni S/D contacts were lithographically patterned on InAs nanoribbons, followed by the atomic layer deposition of ~8-nm-thick ZrO_2 ($\varepsilon \approx 20$) as the gate dielectric. A local top-gate (Ni, 50 nm thick), underlapping the S/D electrodes by ~100 nm, was then lithographically patterned. Importantly, thermal oxidation of InAs was found to significantly improve the interfacial properties and FET characteristics (Supplementary Fig. 8). In this regard, before the S/D contact formation, the XOI substrates were first treated with 3% NH_4OH to remove the native oxide, followed by the thermal oxidation at 350 °C for 1 min to form an ~1-nm-thick $InAsO_x$ layer (as observed from TEM analysis; Fig. 2c).

Figure 4a shows a typical I_{DS}–V_{GS} characteristic of such a top-gated FET, which consists of an individual ~18-nm-thick InAs nanoribbon with a width of ~320 nm. The XOI FET exhibits a respectable on/off current ratio of 10^4, a subthreshold swing of $SS = dV_{GS}/d(\log I_{DS}) \approx 150$ mV per decade (Fig. 4a), and a peak $g_m \approx 1.6$ mS μm^{-1} at $V_{DS} = 0.5$ V (Supplementary Fig. 9). The lowest measured SS for our XOI FETs is ~107 mV per decade (Supplementary Fig. 10), as compared to InAs and InGaAs quantum-well FETs in the literature which have exhibited SS values of ~70 and 75 mV per decade, respectively[10,23]. The devices reported here use a relatively thick gate dielectric, which could be scaled down in the future to further improve the gate electrostatic control and the SS characteristics. The single nanoribbon transistor output characteristic is shown in Fig. 4b, delivering an impressive 'on' current of 1.4 mA μm^{-1} at an operating voltage $V_{DD} = V_{DS} = V_{GS} = 1$ V. To further analyse the performance, a full device simulation was carried out. A close match to the experimental data was obtained with fitting parameter $D_{it} = 10^{11}$ states cm^{-2} eV^{-1} (Supplementary Fig. 7), which is a ~60× improvement over devices without any surface treatment (that is, with a native oxide layer). The fitted D_{it} values represent only estimates. Note that while capacitance–voltage (C–V) measurement is conventionally used for D_{it} extraction in Si devices, doing so is rather challenging and prone to a large uncertainty for narrow-bandgap semiconductors, such as InAs (ref. 26). In the future, the development of more accurate techniques for D_{it} measurement in InAs XOI devices is needed. The explored thermal oxidation process for surface passivation is counter-intuitive, as previous work has focused on the removal of surface oxides[7]. We speculate that unlike the native oxide layer, thermal oxidation results in the formation of a dense oxide with minimal dangling bonds. Similar to thermally grown SiO_2, the thermal oxide of InAs provides an ideal

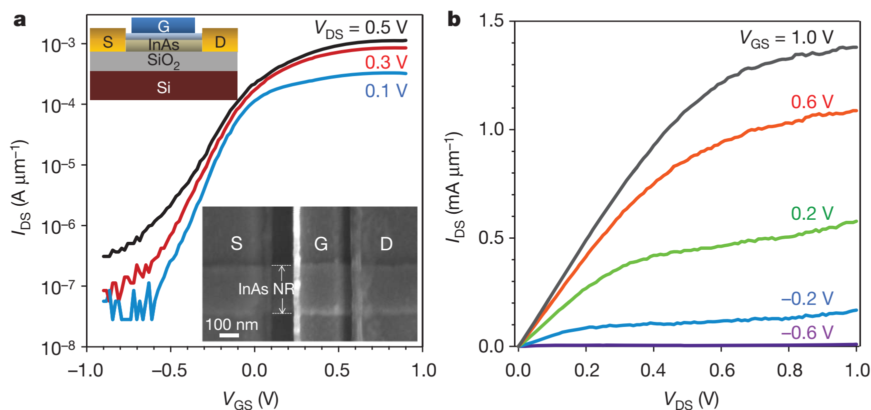

Figure 4 | Top-gated InAs XOI FETs. a, Transfer characteristics of a top-gated InAs XOI FET, consisting of an individual nanoribbon (~18 nm thick) with $L \approx 0.5$ μm and an 8-nm-thick ZrO_2 gate dielectric. Inset, device schematic (top) and a representative SEM image (bottom) of a top-gated FET. NR, nanoribbon. **b**, Output characteristics of the same device shown in **a**. nanoribbons were thermally oxidized at 350 °C for 1 min to form ~1-nm-thick interfacial $InAsO_x$ layer for surface passivation of InAs.

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and simple surface passivation layer, addressing one of the important challenges in InAs devices.

We have demonstrated a new technology platform and device concept for the integration of ultrathin layers of III–V semiconductors directly on Si substrates, enabling excellent electronic device performance. Although in this work we have focused on InAs as the active channel material, other compound semiconductors could be explored in the future, using a similar scheme. Future research on the scalability of the process for 8-inch and 12-inch wafer processing is needed. We suggest that the direct bonding of Si/SiO_2 and III–V wafers, followed by the etch release of the sacrificial layer, might be used in the future to manufacture ultrathin XOI devices on the wafer-scale.

METHODS SUMMARY

Single-crystal InAs thin films (10–100 nm thick) were grown epitaxially on a 60-nm-thick $Al_{0.2}Ga_{0.8}Sb$ layer on bulk GaSb substrates (Supplementary Fig. 1). Polymethylmethacrylate (PMMA) patterns with a pitch and line-width of ~840 nm and ~350 nm, respectively, were lithographically patterned on the surface of the source substrate. The InAs layer was then pattern etched into nanoribbons using a mixture of citric acid (1 g per ml of water) and hydrogen peroxide (30%) at 1:20 volume ratio, which was chosen for its high selectivity and low resulting InAs edge roughness[27]. To release the InAs nanoribbons from the source substrate, the AlGaSb sacrificial layer was selectively etched by ammonium hydroxide (3% in water) solution for 110 min (ref. 28). Note that the selective etch rate of the AlGaSb layer was high enough not to affect the nanoscale structure of the InAs nanoribbons (Supplementary Fig. 2). Next, an elastomeric polydimethylsiloxane (PDMS) substrate (~2 mm thick) was used to detach the partially released InAs nanoribbons from the GaSb donor substrates and transfer them onto Si/SiO_2 (50 nm, thermally grown) receiver substrates by a stamping process (Supplementary Figs 3, 4)[29]. Notably, in this process scheme, the initial epitaxial growth process is used to control the thickness of the transferred InAs nanoribbons, while the lithographically defined PMMA etch mask is used to tune the length and width.

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Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

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Author Contributions H.K., K.T. and A.J. designed the experiments. H.K., K.T., S.C., H.F., E.P., H.S.K., M.M. and A.C.F. carried out the experiments. R.K. and P.W.L. performed device simulations. K.G. and S.S. performed mobility calculations. S.-Y.C. and Y.-L.C. performed TEM imaging. H.K., K.T., R.K., P.W.L., K.G., S.K., S.S. and A.J. contributed to analysing the data. H.K., K.T., R.K. and A.J. wrote the paper while all authors provided feedback.

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